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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/607,274	06/27/2003	Satoshi Seo	60188-566	4710

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EXAMINER	
NGUYEN, KHIEM D	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 10/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/607,274	SATOSHI SEO	
	Examiner	Art Unit	
	Khiem D Nguyen	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 August 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

The drawings were received on August 4th, 2004. These drawings are accepted by the Examiner.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over the applicant's admitted prior art (AAPA) of this application in view of Wakabayashi (U.S. Patent 6,607,970).

In re claim 1, **AAPA** discloses a method for fabricating a semiconductor device, the method comprising the steps of (Background of the invention, pages 1-2 and **FIGS. 20A-22**): (a) forming bonding pads **(FIG. 20A: 304)** above a wafer **(FIG. 20A: 302)** on which semiconductor elements (not shown) and an interconnect layer (not shown) are formed (page 1, lines 10-16); (b) forming a passivation film **(FIG. 20A: 306)** having apertures **(FIG. 20A: 306a and 306b)** including regions of the passivation film located above parts of the bonding pads after the step (a) (page 1, lines 16-21); (c) forming a buffer coat film **(FIG. 20B: 308)** for covering part of the passivation film after the step (b); (d) forming, in the buffer coat film, apertures **(FIG. 20B: 308a)** including regions of the buffer coat film located above scribe line regions and above the parts of the bonding

pads, respectively (page 1, line 22 to page 2, line 5); (e) bonding a surface protection tape **(FIG. 21A: 312)** to the wafer using an adhesive material **(FIG. 21A: 320)** after the step (d) (page 2, lines 2-5); and (f) polishing the rear surface of the wafer after the step (e) **(FIG. 21B: polishing slurry)** (page 2, lines 6-14).

AAPA does not explicitly disclose forming, in the buffer coat film, apertures including regions of the buffer coat film located above a periphery region having a certain distance from the periphery of the wafer, above scribe line regions and above the parts of the bonding pads, respectively.

Wakabayashi discloses a method for fabricating a semiconductor device, the method comprising the steps of: (a) forming bonding pads **(FIG. 7: 2)** above a wafer **(FIG. 7: 1)** on which semiconductor elements and an interconnect layer are formed (col. 3, lines 21-48); (b) forming a passivation film **(FIG. 7: 3)** having apertures **(FIG. 1: 4)** including regions of the passivation film located above parts of the bonding pads after the step (a) (col. 3, lines 37-48); (c) forming a buffer coat film for covering part of the passivation film after the step (b) (col. 3, lines 21-48); (d) forming, in the buffer coat film, apertures **(FIG. 7: 12)** including regions of the buffer coat film located above a periphery region having a certain distance from the periphery of the wafer, above scribe line regions **(FIG. 2: 7)** and above the parts of the bonding pads, respectively (col. 3, lines 38-48); (e) bonding a surface protection tape **(FIG. 7: 14)** to the wafer using an adhesive material **(FIG. 7: 13)** after the step (d) (col. 3, line 64 to col. 4, line 27). It would have been obvious to one of ordinary skill in the art of making semiconductor devices to combine the teaching of AAPA and Wakabayashi to enable the process of

forming, in the buffer coat film, apertures including regions of the buffer coat film located above a periphery region having a certain distance from the periphery of the wafer, above scribe line regions and above the parts of the bonding pads of AAPA to be performed and furthermore to prevent water or moisture from entering the interface between the insulating film 3 (protective film) and the seal film 13 and may oxidize the wirings 5 and the like. Moreover, a crack hardly develops in the interface between the insulation film 3 and the seal film 13 (col. 4, lines 36-43).

In re claim 2, **Wakabayashi** discloses wherein in the step (c), the buffer coat film is formed using a positive-type photosensitive material, and the step (d) includes a process for exposing part of the buffer coat film located on the periphery region of the wafer (col. 3, lines 38-48 and **FIG. 3**). Alternatively, AAPA disclose wherein the buffer coat film is formed using a positive-type photosensitive material (page 1, lines 22-24).

In re claim 3, **Wakabayashi** discloses wherein in the step (c), the buffer coat film is formed using a positive-type photosensitive material, and the step (d) includes a process for exposing part of the buffer coat film located on the wholes of chip regions at least partly overlapped with the periphery region of the wafer (col. 3, lines 38-48 and **FIG. 3**).

In re claim 4, **AAPA** and **Wakabayashi** disclose wherein in the step (c), the buffer coat film is formed using an organic resin, and the step (d) includes a process for selectively removing part of the buffer coat film located on the periphery region of the wafer by a solvent (AAPA, page 1, lines 22-24 and **FIGS. 21A-B**) Wakabayashi (col. 3, lines 38-48 and **FIG. 3**).

In re claim 5, **AAPA** and **Wakabayashi** discloses wherein in the step (c), the buffer coat film is formed using an organic resin, and the step (d) includes a process for blowing gas on part of the buffer coat film located on the periphery region of the wafer before the curing of the buffer coat film (AAPA, page 1, lines 22-24 and **FIGS. 21A-B**) Wakabayashi (col. 3, lines 38-48 and **FIG. 3**).

2. Claims 6-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over the applicant's admitted prior art (AAPA) of this application in view of Wakabayashi (U.S. Patent 6,607,970).

In re claims 6, 8, 9, 11, and 12, **AAPA** discloses a method for fabricating a semiconductor device, the method comprising the steps of (Background of the invention, pages 1-2 and **FIGS. 20A-22**): (a) forming bonding pads **(FIG. 20A: 304)** above a wafer **(FIG. 20A: 302)** on which semiconductor elements (not shown) and an interconnect layer (not shown) are formed (page 1, lines 10-16); (b) forming a passivation film **(FIG. 20A: 306)** having apertures **(FIG. 20A: 306a and 306b)** including regions of the passivation film located above parts of the bonding pads after the step (a) (page 1, lines 16-21); (c) forming a buffer coat film **(FIG. 20B: 308)** for covering part of the passivation film after the step (b); (d) forming, in the buffer coat film, apertures **(FIG. 20B: 308a)** including regions of the buffer coat film located above scribe line regions and above the parts of the bonding pads, respectively (page 1, line 22 to page 2, line 5); (e) bonding a surface protection tape **(FIG. 21A: 312)** to the wafer using an adhesive material **(FIG. 21A: 320)** after the step (d) (page 2, lines 2-5); and (f) polishing the rear surface of the wafer after the step (e) **(FIG. 21B: polishing slurry)** (page 2, lines 6-14).

AAPA does not explicitly disclose forming, in the buffer coat film, apertures including regions of the buffer coat film located above scribe line regions and above the parts of the bonding pads, respectively, and reducing the thickness of part of the buffer coat film located on a periphery region of the wafer having a certain distance from the periphery of the wafer.

Wakabayashi discloses a method for fabricating a semiconductor device, the method comprising the steps of: (a) forming bonding pads **(FIG. 7: 2)** above a wafer **(FIG. 7: 1)** on which semiconductor elements and an interconnect layer are formed (col. 3, lines 21-48); (b) forming a passivation film **(FIG. 7: 3)** having apertures **(FIG. 1: 4)** including regions of the passivation film located above parts of the bonding pads after the step (a) (col. 3, lines 37-48); (c) forming a buffer coat film for covering part of the passivation film after the step (b) (col. 3, lines 21-48); (d) forming, in the buffer coat film, apertures **(FIG. 7: 12)** including regions of the buffer coat film located above scribe line regions **(FIG. 2: 7)** and above the parts of the bonding pads with connection parts connecting between chip regions left among the apertures, respectively, and reducing the thickness of part of the buffer coat film located on a periphery region of the wafer having a certain distance from the periphery of the wafer (col. 3, lines 38-48); (e) bonding a surface protection tape **(FIG. 7: 14)** to the wafer using an adhesive material **(FIG. 7: 13)** after the step (d) (col. 3, line 64 to col. 4, line 27). It would have been obvious to one of ordinary skill in the art of making semiconductor devices to combine the teaching of AAPA and Wakabayashi to enable the process of forming, in the buffer coat film, apertures including regions of the buffer coat film located above scribe line regions and

above the parts of the bonding pads, respectively, and reducing the thickness of part of the buffer coat film located on a periphery region of the wafer having a certain distance from the periphery of the wafer of AAPA to be performed and furthermore to prevent water or moisture from entering the interface between the insulating film 3 (protective film) and the seal film 13 and may oxidize the wirings 5 and the like. Moreover, a crack hardly develops in the interface between the insulation film 3 and the seal film 13 (col. 4, lines 36-43).

In re claims 7-9, **AAPA** discloses wherein bonding a surface protection tape to the wafer using an adhesive paste having a thickness of 15 μm (page 2, lines 2-5) but does not explicitly disclose the thickness range as recited by the Applicants. However, there is no evidence indicating that the reducing thickness of part of the buffer coat film, the thickness of the adhesive paste, and the range of a viscosity of the polishing slurry is critical and it has been held that it is not inventive to discover the optimum or workable ranges of a result-effective variable within given prior art conditions by routine experimentation. See MPEP§2144.05. Note that the specification contains no disclosure of either the critical nature of the claimed dimensions of any unexpected results arising there from. Where patentability is aid to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

In re claim 10, **AAPA** discloses wherein the polishing slurry includes polyethylene glycol (page 2, lines 6-10).

Response to Applicant's Amendment and Arguments

Applicant's arguments filed August 4th, 2004 have been fully considered but they are not persuasive.

Applicants contend that the Examiner admits that AAPA does not disclose the claimed buffer coat film and thereby relies on the teachings of Wakabayashi in an attempt to modify the buffer coat film of AAPA so as to reach the claimed invention.

In response to Applicant's contention that the Examiner admits that AAPA does not disclose the claimed buffer coat film, Examiner respectfully disagrees. Applicants are directed to the Office Action No. 043004 mailed on May 4th, 2004, page 3, 1st paragraph, where the Examiner stated that AAPA teaches forming a buffer coat film 308 for covering part of the passivation film 306 after the step (b) and forming in the buffer coat film, apertures 208a including regions of the buffer coat film located above scribe line regions 310 and above the parts of the boding pads 304 (page 1, line 22 to page 2, line 5, Specification).

The Examiner only admited that AAPA does not explicitly disclose the apertures including regions of the buffer coat film located above a periphery region having a certain distance from the periphery of the wafer. The Examiner thereby combined AAPA and Wakabayashi in order to enable the process of forming, in the buffer coat film, apertures including regions of the buffer coat film located above a periphery region having a certain distance from the periphery of the wafer to be performed. Since the Applicants did not expressly described where the periphery region is located on the wafer in the claimed invention, Examiner taking the broadest definition that the periphery of the

wafer is the edge of the wafer. Thus, the apertures 12 including regions of the buffer coat film located above a periphery region having a certain distance from the periphery of the wafer (FIG. 7, Wakabayashi). Furthermore, as shown in the Specification on page 2, lines 20+ and FIG. 21B, the AAPA by itself could also discloses the step of forming, in the buffer coat film 308, apertures 308a including regions of the buffer coat film located above the periphery region having a certain distance from the periphery of the wafer 302, above scribe line regions 310 and above the parts of the bonding pads 304, respectively.

For these reasons, examiner holds the rejection proper.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D Nguyen whose telephone number is (571) 272-1865. The examiner can normally be reached on Monday-Friday (8:00 AM - 5:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (571) 272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

K.N.
October 25th, 2004

W. DAVID COLEMAN
PRIMARY EXAMINER